# Industrial concurrency specification for C/C++

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# It is time for mechanised industrial standards

Specifications are written in English prose: this is insufficient

Write mechanised specs instead (formal, machine-readable, executable)

Designers can scrutinise, research questions can be identified

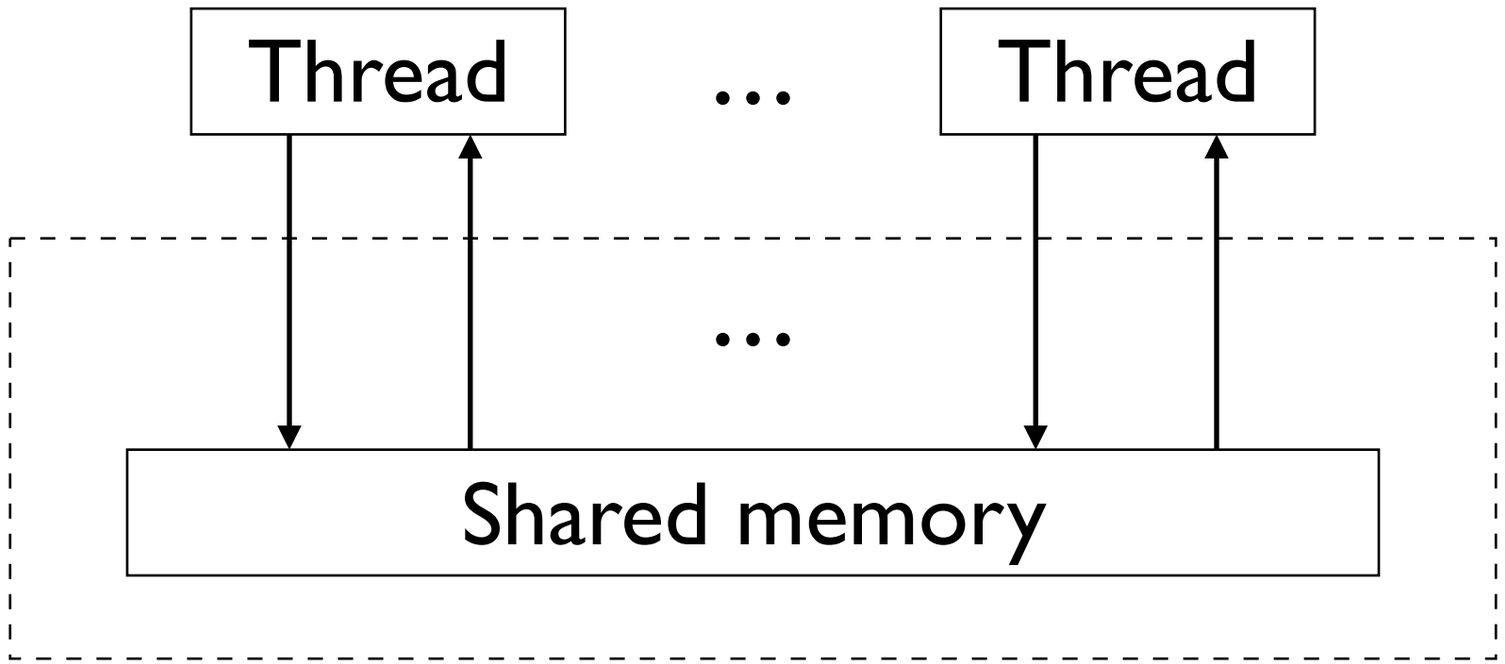
Mechanised specs enable verification for secure systems

Writing mechanised specifications is practical now

# A case study:
# industrial concurrency specification

# Shared memory concurrency

Multiple threads communicate through a shared memory



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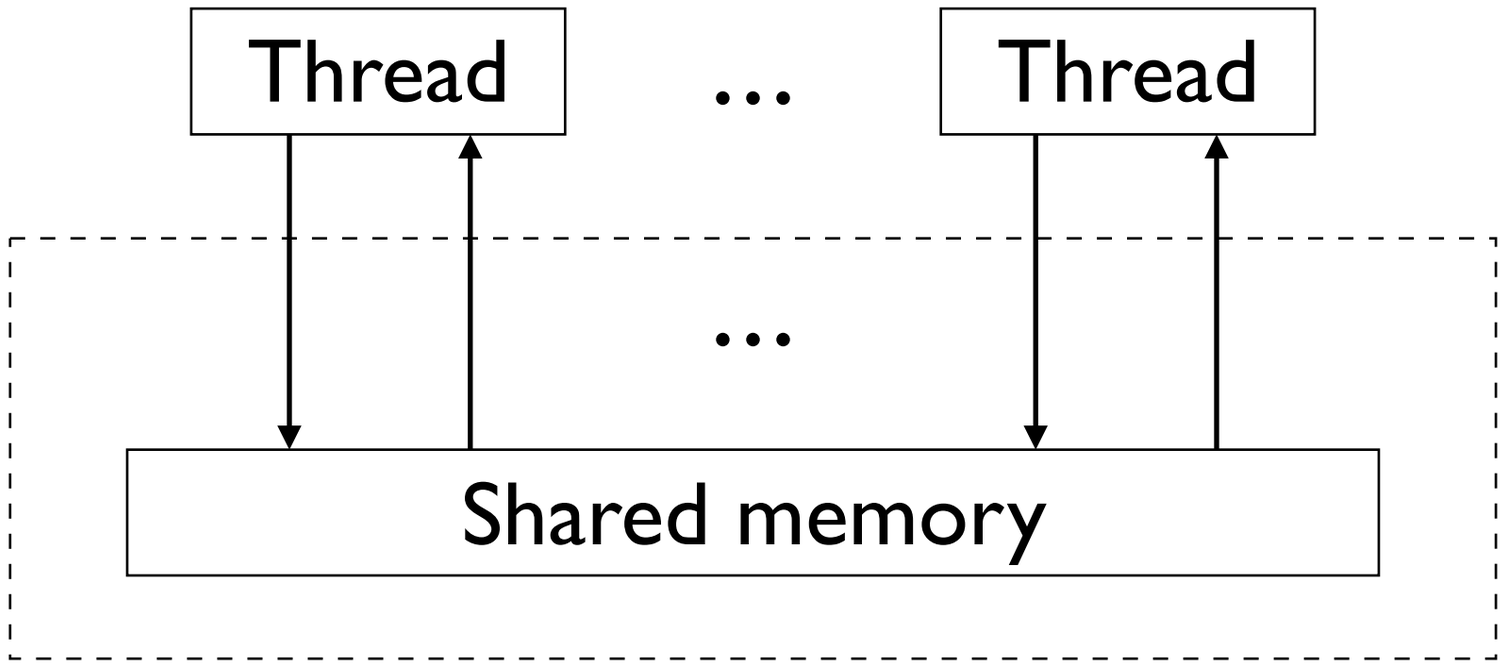


Most systems use a form of shared memory concurrency:

# An example programming idiom

`data`, `flag`, `r` initially zero

Thread 1:

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flag = 1;
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Thread 2:

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while (flag==0)
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r = data;
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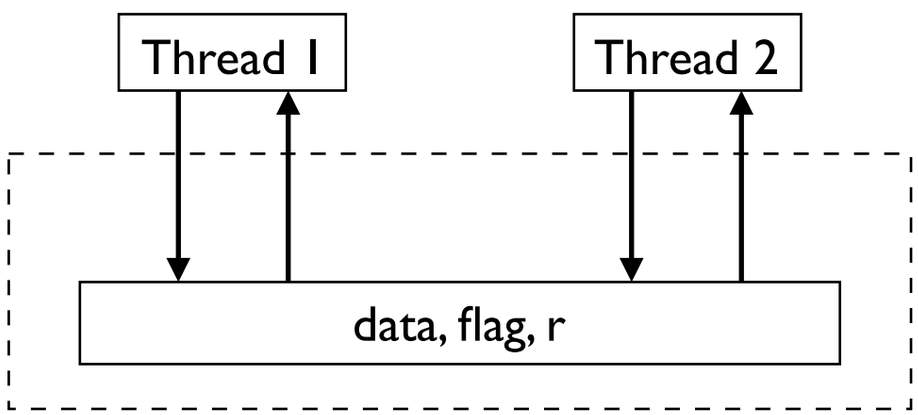
In the end `r==1`




Sequential consistency: simple interleaving of concurrent accesses

Reality: more complex

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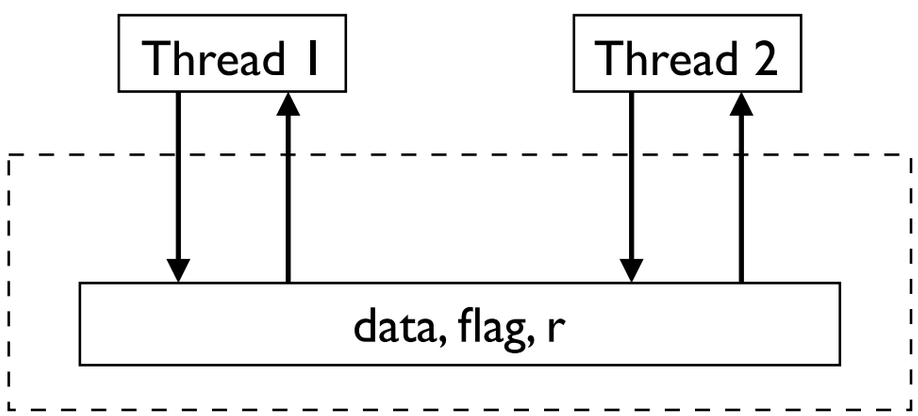


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# Relaxed concurrency

Memory is slow, so it is optimised (buffers, caches, reordering…)

e.g. IBM's machines allow reordering of unrelated writes

(so do compilers, ARM, Nvidia…)

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Many other behaviours like this, some far more subtle, leading to trouble

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# Relaxed behaviour leads to problems

Bugs in deployed processors

Many bugs in compilers

Bugs in language specifications

Bugs in operating systems

Power/ARM processors:
unintended relaxed behaviour
observable on shipped machines

[AMSS10]

# Relaxed behaviour leads to problems

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Errors in key compilers (GCC, LLVM): compiled programs could behave outside of spec.

[MPZN13, CV16]

# Relaxed behaviour leads to problems

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The C and C++ standards had bugs that made unintended behaviour allowed.

More on this later.

[BOS+11, BMN+15]

# Relaxed behaviour leads to problems

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Bugs in operating systems

Confusion among operating system engineers leads to bugs in the Linux kernel

[McK11, SMO+12]

# Relaxed behaviour leads to problems

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Bugs in operating systems

Current engineering practice is severely lacking!

# Vague specifications are at fault

Relaxed behaviours are subtle, difficult to test for and often unexpected, yet allowed for performance

Specifications try to define what is allowed, but English prose is untestable, ambiguous, and hides errors

# A diverse and continuing effort

Modelling of hardware and languages

Simulation tools and reasoning principles

Empirical testing of current hardware

Verification of language design goals

Test and verify compilers

Feedback to industry: specs and test suites

Build mechanised executable formal models of specifications

[AFI+09,BOS+11,BDW16]
[FGP+16,LDGK08,OSP09]
[FSP+17]

# A diverse and continuing effort

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Provide tools to simulate the formal models, to explain their behaviours to non-experts

Provide reasoning principles to help in the verification of code

[BOS+11,SSP+,BDG13]

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Run a battery of tests to understand the observable behaviour of the system and check it against the model

[AMSS'11]

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Explicitly stated design goals should be proved to hold

[BMN+15]

# A diverse and continuing effort

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Feedback to industry: specs and test suites

Test to find the relaxed behaviours introduced by compilers and verify that optimisations are correct

[MPZN13, CV16]

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Feedback to industry: specs and test suites

Specifications should be fixed when problems are found

Test suites can ensure conformance to formal models

[B11]

# A diverse and continuing effort

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Verification of language design goals

Test and verify compilers

Feedback to industry: specs and test suites

## I will describe my part:

# The C and C++ memory model

# Acknowledgements

M. Dodds

A. Gotsman

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S. Owens

J. Pichon-Pharabod

S. Sarkar

P. Sewell

T. Weber

# C and C++

**The** medium for system implementation

Defined by WG14 and WG21 of the International Standards Organisation

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We worked with the ISO, formalising and improving their concurrency design


# C++11 concurrency design

A contract with the programmer: they must avoid **data races**,
two threads competing for simultaneous access to a single variable

`data` initially zero

| Thread 1: | Thread 2: |
| --- | --- |
| `data = 1;` | `r = data;` |

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# Design goals in the standard

The design is complex but the standard claims a powerful simplification:

C++11/14: §1.10p21

It can be shown that programs that correctly use mutexes and `memory_order_seq_cst` operations to prevent all data races and use no other synchronization operations behave [according to] "sequential consistency".

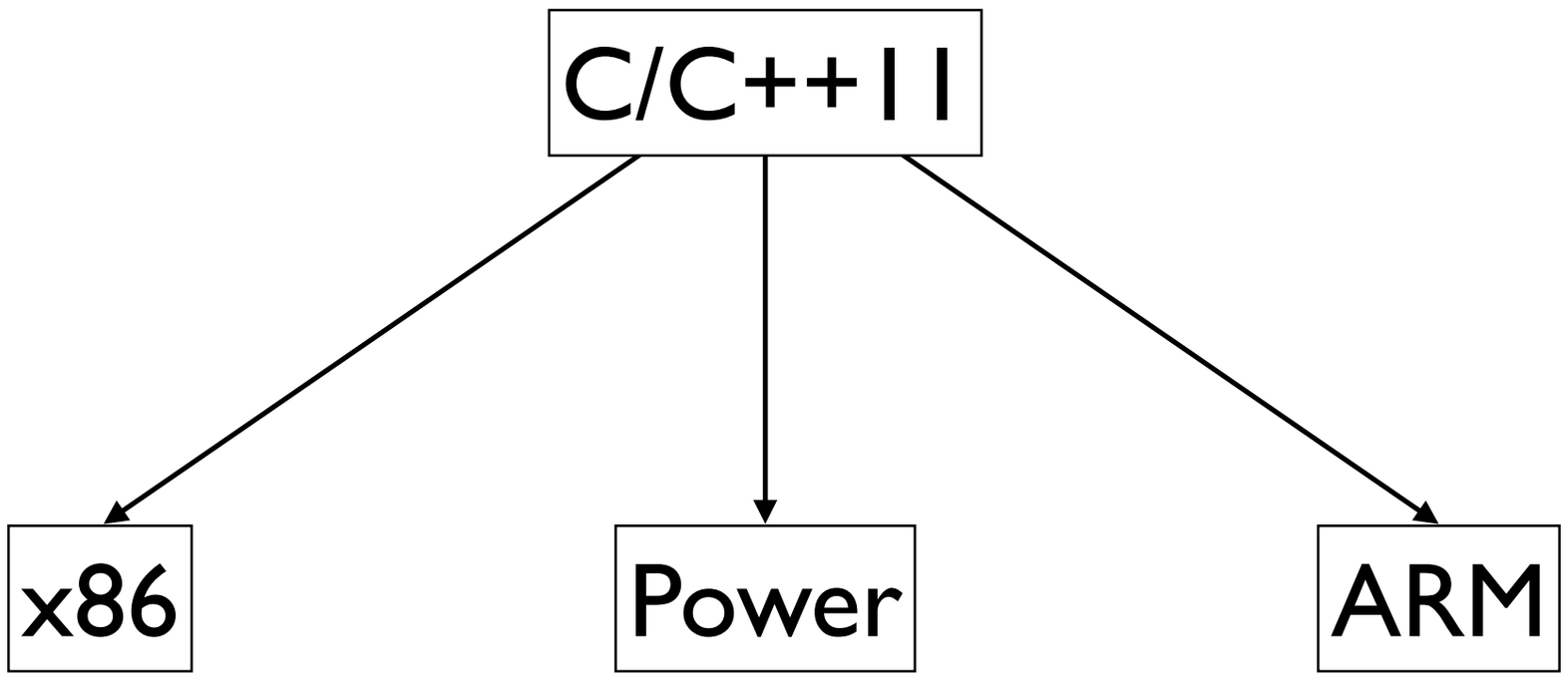
This is the central design goal of the model, called DRF-SC

# Implicit design goals

Compilers like GCC, LLVM map C/C++ to pieces of machine code

| C/C++ | Power | ARM | x86 |
|---|---|---|---|
| Load `acquire` | ld; cmp; bc; isync | ldr; dmb | MOV (from memory) |

Each mapping should preserve the behaviour of the original program



# We formalised a draft of the standard

A mechanised formal model, close to the standard text

## C++11 standard §1.10p12:

An evaluation A happens before an evaluation B if:

- A is sequenced before B, or
- A inter-thread happens before B.

The implementation shall ensure that no program execution demonstrates a cycle in the "happens before" relation.

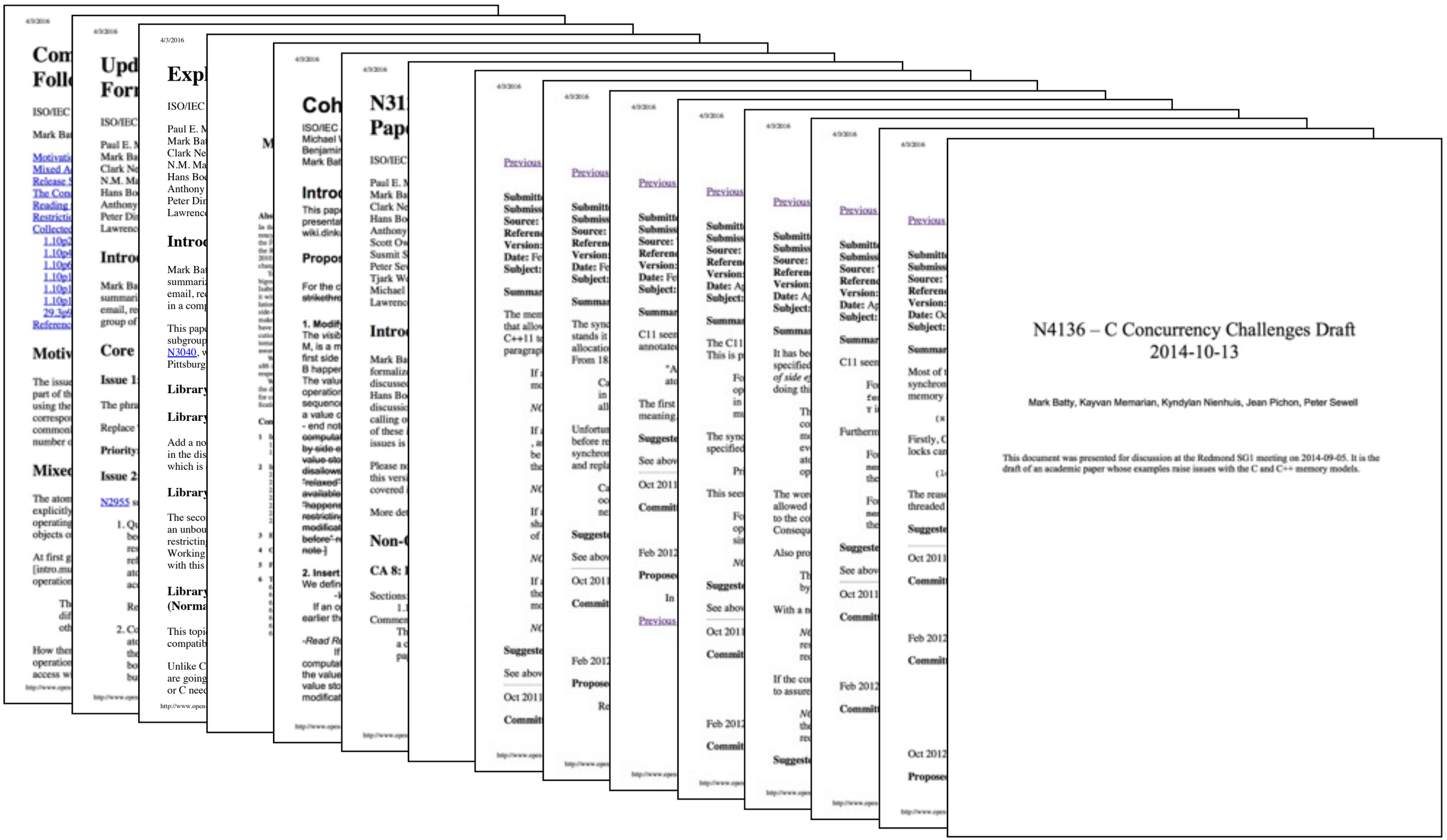
## The corresponding formalisation:

let *happens_before sb ithb* = *sb* ∪ *ithb*

let *consistent_hb hb* =
    isIrreflexive (transitiveClosure *hb*)

# Communication with WG21 and WG14

## Issues were discussed in N-papers and Defect Reports



# Major problems fixed, key properties verified

**DRF-SC:**

The central design goal, was **false**, the standard permitted too much

Fixed the model and then proved (in HOL4) that the goal is now **true**

Fixes were incorporated, pre-ratification, and are in C++11/14

**Compilation mappings:**

Efficient x86, Power mappings are sound [BOS+11,BMO+12,SMO+12]

**Reasoning:**

Developed a reasoning principle for proving programs correct [BDO13]

# Timing was everything

Achieved direct impact on the standard

Making this work was partly a social problem

C++11 was a major revision, so the ISO was receptive to change

But…

# A fundamental problem uncovered

`x`, `y`, `r1`, `r2` initially zero

```
// Thread 1                  // Thread 2
r1 = x;                      r2 = y;
if(r1==1) y = 1;             if(r2==1) x = 1;
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Can we observe `r1==1`, `r2==1` at the end?

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The write of y is dependent on the read of x

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"[ *Note:* […] However, implementations should not allow such behavior. — *end note* ]"

ISO: notes carry no force, and "should" imposes no constraint, so yes!

# A fundamental problem uncovered

**Why?** Dependencies are ignored to allow dependency-removing optimisations

C++ Should respect the left-over dependencies

We have proved that no fix exists in the structure of the current specification

This identifies a difficult research problem

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`1/1` ne

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# The thin-air problem

# A slightly different program

x, y, r1, r2 initially zero

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r1 = x;                      r2 = y;
if(r1==1) y = 1;             if(r2==1) {x = 1}
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Can we observe r1==1, r2==1 at the end?

In both branches on Thread 2, 1 is written to x

An optimising compiler may perform common subexpression elimination

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In the altered program, ARM would allow the outcome `1 / 1`

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Can we observe `r1==1`, `r2==1` at the end?

We need a semantic notion of dependency

Execution depends on more than one control-flow path

C++ spec considers one at a time: fundamental change is needed

# Current work

**Several candidates:**

- The Promising Semantics [KHL+17] — an abstract machine with speculation of writes through *promises*. At each step, promised writes must be sure to execute.

- Jeffrey and Riely [JR16] — based on event structures, executions are built up iteratively, out of order. Add a read only if the write it reads from must be executed.

- Podkopaev, Sergey, and Nanevski [PSN16] — an abstract machine where conditionals can be preemptively explored, and writes that always occur can be promoted.

- Bubbly and Ticky semantics [PPS16] — based on event structures. The event structure is non-deterministically mutated in a transition system that mimics compiler optimisations.

Each relies on a repeated search over multiple control-flow paths

This makes the models more expensive to evaluate than C++ (cannot use SAT)

Which model to choose?

# Model simulation

Simulators provide lightweight automatic validation of design criteria:
[WBSC17] uses SAT to check DRF-SC, compiler mappings, litmus tests for C++, OpenCL, CPUs, GPUs

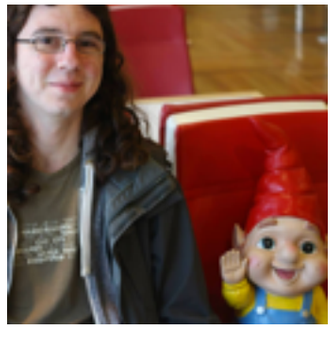
We are building a simulator for thin-air models

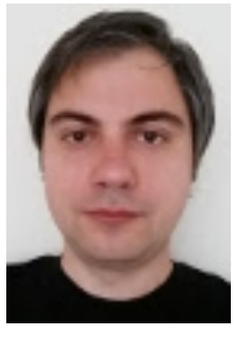
Higher complexity requires advanced Quantified Boolean Formula solvers

A VeTTS grant is paying for the development of a web interface

Our own solution to the thin-air problem is under development:

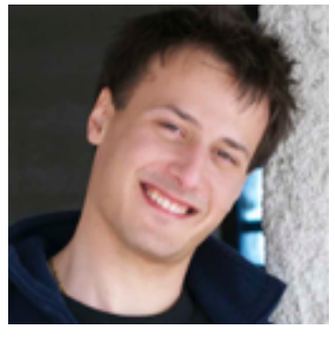
a compositional denotational semantics that looks rather different [B17]


Simon Cooksey


Radu Grigore

University of Kent
Sarah Harris


Scott Owens


Marco Paviotti

# Conclusion

Mechanised industrial specification is practical, with a valuable payoff:

- Improved specs
- Simulators — an executable golden model that matches the spec
- Test suites can be generated
- Design criteria can be validated

It can guide us to future research questions

It is a necessary step in formal verification of security properties

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